Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 10. (Canceled)

11. (New) A semiconductor device, comprising:

a memory cell array having memory cells arranged in rows and columns, said memory cells storing data and being selected according to address signals;

control section configured to receive a clock signal and a control signal, and configured to output a plurality of said data in synchronism with said clock signal after said control signal is asserted, output of said data beginning a number of clock cycles (latency N) of said clock signal (latency N being a positive integer ≥2) after said control signal is asserted, a different one of said data being output at each of said clock cycles after said output begins until said plurality of data is output; and

latency setting circuit configured to set the latency N, said latency setting circuit including at least one switch which fixes the latency by use of an externally supplied signal.

12. (New) The semiconductor device according to claim 11, wherein said latency setting circuit includes a logic circuit which controls said at least one switch based on said externally supplied signal.

13. (New) The semiconductor device according to claim 11, wherein said externally supplied signal includes a command which fixes the latency N, set by said latency setting circuit.

14. (New) The semiconductor device according to claim 11, wherein the memory cells are one of a dynamic memory cell, a static memory cell and a non-volatile memory cell.

15. (New) A semiconductor device comprising:

a memory cell array having memory cells arranged in rows and columns;

a counting circuit configured to receive a clock signal and counting a number of clock cycles of the clock signal;

a control circuit configured to receive an external control signal, and to generate an internal control signal on the basis of the external control signal and/or an output signal from the counting circuit;

a specification circuit configured to receive address signals in response to the internal control signal generated from the control circuit, and to designate a memory cell in said memory cell array;

a selection circuit configured to receive the address signals in response to the internal control signal from said control circuit and an output signal from the specification circuit, and to select one of a normal operation mode and a synchronous mode in a mode setting cycle; and

latency setting circuit configured to set the latency N, said latency setting circuit including at least one switch which permanently fixes a latency,

wherein in the normal mode, the specification circuit sets address signals of the memory cell in the memory cell array, irrespective of the clock signal, and in the synchronous mode, the specification circuit determines a setting timing of the address signals of the memory cell in the memory cell array, in response to the clock signal.

16. (New) The semiconductor device according to claim 15, further comprising a data I/O circuit configured to input data into the memory cell selected by said specification circuit and to output the data from the memory cell selected by said specification circuit.

17. (New) The semiconductor device according to claim 15, wherein said specification circuit determines the setting timing of the address signals of the memory cell

in said memory cell array in synchronism with a rising edge or a falling edge of the clock signal.

18. (New) The semiconductor device according to claim 15, wherein the memory cell is one of a dynamic memory cell, a static memory cell and a non-volatile memory cell.

19. (New) The semiconductor device according to claim 15, wherein the output of data begins a number of clock cycles (latency N) of the clock signal (latency N being a positive integer ≥ 2) after setting of the synchronous mode, a different one of the data being output at each of the clock cycles after the output begins until the plurality of data is output.

20. (New) The semiconductor device according to claim 19, wherein the latency N is determined by externally supplying a latency control signal.

21. (New) The semiconductor device according to claim 19, wherein the latency N is variably programmed.

22. (New) The semiconductor device according to claim 15, wherein the address signals include row address signals and column address signals; and

the external control signal includes a row enable signal for inputting row address signals into the specification circuit and a column enable signal for, after a row address is determined in the specification circuit by an input of the row address signals, inputting the column address signals into the specification circuit.

23. (New) The semiconductor device according to claim 15, wherein the address signals include at least row address signals, and

the external control signal includes at least a row enable signal for inputting row address signals into the specification section.

24. (New) The semiconductor device according to claim 15, wherein the address signals include at least column address signals, and

the external control signal includes at least a column enable signal for inputting column address signals into the specification circuit.

25. (New) The semiconductor device according to claim 15, wherein the counting circuit includes a series of shift registers for transferring a trigger signal in response to a signal synchronized with the clock signal.

26. (New) The semiconductor memory device according to claim 25, wherein each of the shift registers includes clocked inverters which operate in response to the signal synchronized with the clock signal.

27. (New) A semiconductor device comprising:

a memory cell array having memory cells arranged in rows and columns;

a counting circuit configured to receive a clock signal and counting a number of clock cycles of the clock signal;

a control circuit configured to receive an external control signal, and to generate an internal control signal on the basis of the external control signal and/or an output signal from the counting circuit;

a specification circuit configured to receive address signals in response to the internal control signal generated from the control circuit, and to designate a memory cell in said memory cell array;

a selection circuit configured to receive the address signals in response to the internal control signal from said control circuit and an output signal from the specification circuit, and to select one of a normal operation mode and a synchronous mode in a mode setting cycle; and

latency setting circuit configured to set the latency N, said latency setting circuit including at least one switch which fixes the latency based on an externally supplied signal,

wherein in the normal mode, the specification circuit sets address signals of the memory cell in the memory cell array, irrespective of the clock signal, and in the synchronous mode, the specification circuit determines a setting timing of the address signals of the memory cell in the memory cell array, in response to the clock signal.

28. (New) The semiconductor device according to claim 27, further comprising a data I/O circuit configured to input data into the memory cell selected by said specification circuit and to output the data from the memory cell selected by said specification circuit.

29. (New) The semiconductor device according to claim 27, wherein said specification circuit determines the setting timing of the address signals of the memory cell in said memory cell array in synchronism with a rising edge or a falling edge of the clock signal.

30. (New) The semiconductor device according to claim 27, wherein the memory cell is one of a dynamic memory cell, a static memory cell and a non-volatile memory cell.

31. (New) The semiconductor device according to claim 27, wherein the output of data begins a number of clock cycles (latency N) of the clock signal (latency N being a positive integer ≥ 2) after setting of the synchronous mode, a different one of the data being output at each of the clock cycles after the output begins until the plurality of data is output.

32. (New) The semiconductor device according to claim 27, wherein the address signals include row address signals and column address signals; and

the external control signal includes a row enable signal for inputting row address signals into the specification circuit and a column enable signal for, after a row address is determined in the specification circuit by an input of the row address signals, inputting the column address signals into the specification circuit.

33. (New) The semiconductor device according to claim 27, wherein the address signals include at least row address signals, and

the external control signal includes at least a row enable signal for inputting row address signals into the specification section.

34. (New) The semiconductor device according to claim 27, wherein the address signals include at least column address signals, and

the external control signal includes at least a column enable signal for inputting column address signals into the specification circuit.

35. (New) The semiconductor device according to claim 27, wherein the counting circuit includes a series of shift registers for transferring a trigger signal in response to a signal synchronized with the clock signal.

36. (New) The semiconductor memory device according to claim 35, wherein each of the shift registers includes clocked inverters which operate in response to the signal synchronized with the clock signal.